CLAIMS

1. An integrated circuit, comprising:

a switch;

a capacitor; and

a nonconductive oxygen barrier located between said switch and said capacitor.

2. An integrated circuit as in claim 1 wherein said oxygen barrier comprises strontium tantalate.

3. An integrated circuit as in claim 2 wherein said oxygen barrier further comprises silicon nitride.

4. An integrated circuit as in claim 1 wherein said capacitor comprises a bottom electrode having a bottom-electrode side edge, and at least a portion of said oxygen barrier is located on said bottom-electrode side edge.

5. An integrated circuit as in claim 4, further comprising:

a conductive diffusion barrier comprising a conductive-barrier side edge, said bottom electrode being located on said conductive diffusion barrier; and wherein at least a portion of said oxygen barrier is located on said conductive-barrier side edge.

6. An integrated circuit as in claim 5, further comprising:

an insulator layer located between said switch and said capacitor, said conductive diffusion barrier being located on a portion of said insulator layer, and a portion of said oxygen barrier being located on said insulator layer.

7. An integrated circuit as in claim 6 wherein said insulator layer comprises a moat region, said moat region being defined partially by a moat sidewall and a moat bottom, said moat region being substantially coplanar with said bottom electrode and said conductive diffusion barrier, said moat bottom comprising a portion of said oxygen barrier, and said moat sidewall comprising a portion of said oxygen barrier.

8. An integrated circuit as in claim 7 wherein said insulator layer comprises an over-etched portion aligned with said conductive- barrier side edge, and wherein said bottom-electrode side edge, said conductive-barrier side edge, and said over-etched portion define a moat sidewall, and at least a portion of said

oxygen barrier layer is located on said bottom-electrode side edge, said conductive-barrier side edge, and said over-etched portion.

9. An integrated circuit as in claim 6 wherein said conductive diffusion barrier and said oxygen barrier together substantially completely cover said switch.

10. An integrated circuit as in claim 6 wherein said conductive diffusion barrier and said oxygen barrier together form a substantially continuous diffusion barrier between said capacitor and said switch.

11. An integrated circuit as in claim 6, further comprising a nonconductive hydrogen barrier layer, said nonconductive hydrogen barrier layer substantially completely covering said capacitor and said switch.

12. An integrated circuit as in claim 11 wherein said nonconductive hydrogen barrier layer comprises strontium tantalate.

13. An integrated circuit as in claim 12 wherein said nonconductive hydrogen barrier layer further comprises silicon nitride.

14. An integrated circuit as in claim 11 wherein said capacitor comprises a top electrode, and a portion of said nonconductive hydrogen barrier layer is located on said top electrode.

15. An integrated circuit as in claim 11 wherein said capacitor comprises a top plate-line electrode, and a portion of said nonconductive hydrogen barrier layer is located on said plate-line electrode.

16. An integrated circuit as in claim 15, further comprising an electrical connection to said top plate-line electrode, said electrical connection located remotely from said capacitor.

17. An integrated circuit as in claim 11 wherein said top electrode comprises a top-electrode side edge, and a portion of said nonconductive hydrogen barrier layer is located on said top-electrode side edge.

18. An integrated circuit as in claim 11 wherein said capacitor comprises a capacitor dielectric film comprising a capacitor-dielectric side edge, and a portion of said nonconductive hydrogen barrier layer is located on said capacitor-dielectric side edge.

19. An integrated circuit as in claim 5 wherein said conductive barrier layer comprises titanium aluminum nitride.

20. An integrated circuit as in claim 1, further comprising a nonconductive hydrogen barrier layer, said nonconductive hydrogen barrier layer substantially completely covering said capacitor and said switch.

21. An integrated circuit as in claim 20, further comprising a non-memory portion, said non-memory portion not being covered by said hydrogen barrier layer.

22. An integrated circuit as in claim 20 wherein said nonconductive hydrogen barrier layer comprises strontium tantalate.

23. An integrated circuit as in claim 22 wherein said nonconductive hydrogen barrier layer further comprises silicon nitride.

24. An integrated circuit as in claim 1 wherein said capacitor comprises a thin film of ferroelectric layered superlattice material.

25. An integrated circuit as in claim 24 wherein said thin film comprises ferroelectric layered superlattice material selected from the group consisting of strontium bismuth tantalate and strontium bismuth tantalum niobate.

26. An integrated circuit as in claim 25 wherein said thin film has a thickness not exceeding 90 nm.

27. An integrated circuit comprising:

an element sensitive to degradation by oxygen; and

a nonconductive oxygen barrier layer located to protect said element, said oxygen barrier layer comprising strontium tantalate.

28. An integrated circuit as in claim 27 wherein said oxygen barrier layer further comprises silicon nitride.

29. An integrated circuit as in claim 27, further comprising an electrically conductive diffusion barrier located proximate to said oxygen barrier layer, said conductive diffusion barrier and said oxygen barrier together forming a substantially continuous diffusion barrier to protect said element.

30. A method of fabricating a memory cell, comprising steps of:

providing a substrate, said substrate comprising a switch, an insulator layer covering said switch, and a conductive plug, said conductive plug having a bottom end and a top end, said bottom end in electrical connection with said switch;

thereafter forming a conductive diffusion barrier layer and a bottom electrode layer on said substrate;

then removing a portion of said bottom electrode layer, of said conductive diffusion barrier layer, and of said insulator layer, thereby forming a bottom electrode, a conductive diffusion barrier, and an over-etched portion of said insulator layer, said conductive diffusion barrier having a conductive-barrier side edge and being located on said top end of said conductive plug, said bottom electrode having a bottom-electrode side edge and being located on said conductive diffusion barrier;

whereby said removing said portion of said insulator layer forms said over-etched portion of said insulator layer and a moat space adjacent to said conductive diffusion barrier and said bottom electrode, said moat space being partially defined by a moat bottom and a moat sidewall, whereby said moat sidewall comprises said bottom-electrode side edge, said conductive-barrier side edge, and said over-etched portion of said insulator layer.

31. A method as in claim 30, further comprising a step of forming a nonconductive oxygen barrier layer on said substrate.

32. A method as in claim 31 wherein said forming said oxygen barrier layer comprises depositing a portion of said oxygen barrier layer on said bottom-electrode side edge.

33. A method as in claim 31 wherein said forming said oxygen barrier layer comprises depositing a portion of said oxygen barrier layer on said conductive-barrier side edge.

34. A method as in claim 31 wherein said forming said oxygen barrier layer comprises depositing a portion of said oxygen barrier layer on said over-etched portion of said moat sidewall.

35. A method as in claim 31 wherein said forming said oxygen barrier layer comprises depositing a portion of said oxygen barrier layer on said bottom-electrode side edge, on said conductive-barrier side edge, and on said over-etched portion of said moat sidewall.

36. A method as in claim 31 wherein said forming said oxygen barrier layer comprises depositing a portion of said oxygen barrier layer on said insulator layer.

37. A method as in claim 36 wherein said forming said oxygen barrier

layer comprises depositing a portion of said oxygen barrier layer on said moat bottom.

38. A method as in claim 31 wherein said forming said oxygen barrier layer comprises depositing said oxygen barrier layer such that said oxygen barrier and said conductive diffusion barrier together substantially completely cover said switch.

39. A method as in claim 31 wherein said forming said oxygen barrier layer comprises forming said oxygen barrier layer proximate to said conductive diffusion barrier such that said oxygen barrier layer and said conductive diffusion barrier together constitute a substantially continuous diffusion barrier between said bottom electrode and said switch.

40. A method as in claim 31 wherein said forming said oxygen barrier layer comprises depositing strontium tantalate.

41. A method as in claim 40 wherein said forming said oxygen barrier layer comprises depositing silicon nitride.

42. A method as a claim 31, further comprising steps of:

forming a capacitor dielectric layer and a top electrode layer on said substrate;

forming a memory capacitor on said substrate; and

thereafter depositing a nonconductive hydrogen barrier layer on said substrate, said hydrogen barrier layer substantially completely covering said memory capacitor and said switch.

43. A method as in claim 42 wherein said step of depositing a nonconductive hydrogen barrier layer comprises depositing strontium tantalate.

44. A method as in claim 42 wherein said step of depositing a nonconductive hydrogen barrier layer further comprises depositing silicon nitride.

45. A method as in claim 42 wherein said forming a memory capacitor comprises removing a portion of said top electrode layer to form a top electrode, and said depositing a nonconductive hydrogen barrier layer comprises depositing a portion of said nonconductive hydrogen barrier layer on said top electrode.

46. A method as in claim 42 wherein said forming a memory capacitor comprises removing a portion of said top electrode layer to form a top plate-line

electrode, and said depositing a nonconductive hydrogen barrier layer comprises depositing a portion of said nonconductive hydrogen barrier layer on said plate-line electrode.

47. A method as in claim 46 wherein said forming a memory capacitor comprises forming a top plate-line electrode having a top-electrode side edge, and said depositing a nonconductive hydrogen barrier layer comprises depositing a portion of said nonconductive hydrogen barrier layer on said top-electrode side edge.

48. A method as in claim 42 wherein said forming a memory capacitor comprises removing a portion of said capacitor dielectric layer to form a capacitor dielectric film having a capacitor-dielectric side edge, and said depositing a nonconductive hydrogen barrier layer comprises depositing a portion of said nonconductive hydrogen barrier layer on said capacitor-dielectric side edge.

49. A method as in claim 48, further comprising a step of removing a non-memory portion of said nonconductive hydrogen barrier layer from said substrate.

50. A method as a claim 42 wherein said forming of said dielectric layer comprises depositing metal oxide precursor material for forming ferroelectric layered superlattice material.

51. A method as in claim 50 wherein said forming said dielectric layer comprises forming a layered superlattice material selected from the group consisting of strontium bismuth tantalate and strontium bismuth tantalum niobate.

52. A method as in claim 50 wherein said forming said dielectric layer comprises heating said precursor material using RTP at a temperature in a range of about from 400°C to 800°C for a total duration comprising less than 30 minutes.

53. A method as in claim 52 wherein said total duration comprises less than 15 minutes.

54. A method as in claim 53 wherein said total duration comprises less than 5 minutes.

55. A method as in claim 50 wherein said forming said dielectric layer comprises forming a thin film of layered superlattice material having a thickness not exceeding 90 nm.